SUPPLEMENTAL *Notice of Allowability*	Application No. 09/696,836	Applicant(s) VANHOOF ET AL.	
	Examiner J. Bret Dennison	Art Unit 2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/18/2005*.

2. ☒ The allowed claim(s) is/are *93-97*.

3. ☒ The drawings filed on *25 October 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *6/5/06* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER

SUPPLEMENTAL EXAMINER'S AMENDMENT

1. An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Bruce Itchkawitz (Reg. # 47,677) on 6/5/2006.

3. The application has been amended as follows:

IN THE SPECIFICATION

Please amend the specification at page 17, lines 4-5 from:

~~Figure 18 illustrates two abstraction levels for C-software code implementation of the IPC protocol on the ARM processor.~~

to read as:

Figures 18A and 18B illustrate two abstraction levels for C-software code implementation of the IPC protocol on the ARM processor.

IN THE CLAIMS

93. A method for defining a system specification for a digital system, said method comprising the steps of:

partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;

defining separately from said processes single data independent data communication protocol for communication within said digital system and between said processes;

configuring data communication interfaces in the form of communication input ports and communication output ports for each of the processes, the communication ports forming memory free communication channels, said step of configuring data communication interfaces involving defining communication interfaces with input ports of a first process and output ports to provide unidirectional, point-to-point connections between input ports of a first process and output ports of a second process, said input ports and said output ports being part of the associated processes, said processes implemented in C, Silage or VHDL language; and

combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.

94. A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said single data independent data communication protocol with input and output ports for said

processes, said ports using memory free communication channels; and

designing a plurality of processors to implement said process, said step of designing ~~desiring~~ processors comprising the step of specifying a processor having specification which conforms to the processes implemented, said processor comprising a programmable digital signal processor, wherein said plurality of specifications are selected from a group consisting of Silage descriptions, C descriptions, VHDL process descriptions.

95. A method of implementing a digital system

comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said single data independent data communication protocol with input and output ports for said processes, said ports using memory free communication channels implemented as interrupt driven I/0; and

designing a plurality of processors to implement said' process, said step of designing ~~desiring~~ processors comprising the step of specifying a processor having specification which conforms to the processes implemented.

96. A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said single data independent data communication protocol with input and output ports for said processes, said ports using memory free communication channels, said communication channels implemented in integrated circuit form for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types, wherein said plurality of processor types consists of Cathedral-III processors, ARM processors and VHDL generated processors; and

designing a plurality of processors to implement said process, said step of designing processors comprising the step of specifying a processor having specification which conforms to the processes implemented, said processor comprising a programmable, general purpose processor.

97. A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread, said step of partitioning involving

defining a library of auxiliary processes to simulate the digital system, the library of processes selected from a plurality of processes consisting of one or more of an interactive I/0 process, a file I/0 process, a graphical output process, a channel duplicator process, a channel merging process, a FF process, a slider process, a button process, a first-in, first-out buffer process, an ARM processor, a digital to analog conversion process and an analog to digital conversion process;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said single data independent data communication protocol with input and output ports for said

processes, said ports using memory free communication channels; and

designing a plurality of processors to implement said process, said step of designing processors comprising the step of specifying a processor having specification which conforms to the processes implemented, wherein said processor comprises a programmable digital signal processor.

Conclusion

4. Please refer to Previous Office Action for Reasons For Allowance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Bret Dennison whose telephone number is (571) 272-3910. The examiner can normally be reached on M-F 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. B. D.
Patent Examiner
Art Unit 2143

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER